



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,432	01/23/2004	Paul Brian Ripy	200-66300 (2003-00900)	6824
56929	7590	06/28/2006	EXAMINER	
LAW OFFICES OF MARK C. PICKERING P.O. BOX 300 PETALUMA, CA 94953			PATEL, HETUL B	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/763,432

Applicant(s)

RIPY ET AL.

Examiner

Hetul Patel

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 May 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7, 8, 10, 12, 16-19 and 21-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 16, 17, 21 and 26 is/are rejected.
- 7) ☒ Claim(s) 4, 7, 8, 10, 12, 18, 19, 22-25 and 27-30 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>05/18/2006</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to communication filed on May 18, 2006. This amendment has been entered and carefully considered. Claims 5-6, 9, 11, 13-15 and 20 are cancelled; claims 1-4, 7-8, 10, 12 and 16-19 are amended; and claims 21-30 are newly added. Therefore, claims 1-4, 7-8, 10, 12, 16-19 and 21-30 are pending in this application.
2. The IDS filed on 05/18/2006 has been received and carefully considered.
3. Applicant's arguments filed on May 18, 2006 have been fully considered but they are not deemed to be moot in view of new ground rule rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 16-17, 21 and 26 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Larson et al. (USPN: 5,481,680) hereinafter, Larson.

As per claims 1 and 3, Larson teaches a method of adding (i.e. the grant bits, G0-G3 in Fig. 7) to a memory (i.e. the memory device 12 in Fig. 1) that stores information about a series of arbitration periods, the method comprising: assigning a number of first addresses (i.e. addresses as shown in the left column in Fig. 7) to a

group of devices (i.e. 14, 16, 18 and 20 in Fig. 1) and no two devices have the same first addresses, the number of first addresses representing a corresponding number of arbitration periods such that each first address represents one arbitration period (e.g. see Col. 3, lines 11-29), each first address having a sequence of bits (i.e. 0000-1111 as shown in Fig. 7); and forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses, each second address representing one arbitration period (i.e. the grant bits G0-G3 in Fig. 7 are assigned to each one of the plurality of logical addresses 0000-1111 of the memory as shown in Fig. 7 and each logical address corresponds to a physical address of the memory spaced apart from the physical address, which is an inherent feature of the method taught by Larson) (e.g. see Col. 5, lines 30+ and Figs. 1, 5-7).

Although Larson does not specifically disclose in Fig. 7 that two or more consecutive first addresses are assigned to each device, Larson does disclose that the Fig. 7 disclose the a block of memory according to a simple "priority" algorithm, however, the arbitration scheme is not required to be the "priority" scheme as shown in Fig. 7 and any other arbitration scheme can be used such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses (e.g. see Col. 5, lines 47-50).

As per claims 21 and 26, see arguments with respect to the rejection of claim 1. Claims 21 and 26 are also rejected based on the same rationale as the rejection of claim 1.

As per claim 2, Larson teaches the claimed invention as described above and furthermore, Larson teaches that the method further comprising for each second address (i.e. the corresponding physical address), writing grant information (i.e. the grant bits, G0-G3 in Fig. 7) to the memory about the corresponding device (e.g. see Fig. 7).

As per claims 16 and 17, Larson teaches a communications circuit as shown in Fig. 1. A transmit circuit for transmitting information onto a bus; a receive circuit for receiving information from the bus; and a logic circuit are inherently embedded in the CPU 14 shown in Fig. 1. Larson also teaches the further claimed limitations of claim 16 and 17 as shown above in the rejection of claim 1.

Allowable Subject Matter

5. Claims 4, 7-8, 10, 12, 18-19, 22-25 and 27-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance:

The prior arts of record do not teach nor suggest, either alone or in combination, the limitation(s) of objected claims, i.e. forming the second addresses from the

corresponding first addresses by setting all bits of the second address equal to the all bits of the corresponding first address in the reverse order.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HBP
HBP



MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100